IN THE CLAIMS

Please amend the currently pending claims as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-47. (Cancelled)

48. (Currently amended) A wafer track system to reduce the effects of thermal crosstalk arising from handling semiconductor wafers with wide-ranging temperature ranges comprising:

a wafer processing section including:

a first wafer process station containing wafer processing stacks of process modules which are positioned along selected portions of a predetermined polygonal configuration substantially surrounding a first main wafer transporter; and

a second wafer process station containing wafer processing stacks of process modules which are positioned along selected portions of a predetermined polygonal configuration substantially surrounding a second main wafer transporter;

a cassette end section (CES) for storing wafer cassettes that is positioned adjacent to each of the wafer process stations, the CES including at least one cassette wafer transporter for transferring semiconductor wafers between the CES and at

least one wafer processing stack associated with each wafer process station; and

a stepper interface section (SI) for enabling external access to the wafer ~~cassettes that is~~ process stations positioned adjacent to each of the wafer process stations, the SI including at least one stepper wafer transporter for transferring semiconductor wafers between the SI and at least one wafer processing stack associated with each wafer process station,

wherein the first and the second main wafer transporters are each configured for transporting semiconductor wafers into a wafer bake module within a wafer processing stack in each respective wafer process station, and wherein one of the cassette and the stepper wafer transporters are configured for transporting semiconductor wafers out of the wafer bake module ~~with~~ within the wafer processing stack for each respective wafer process station.

49. (Previously presented) The wafer track system as recited in claim 48, wherein the first wafer process station and the second wafer process station include at least two process modules which process semiconductor wafers at different wafer processing temperatures.

50. (Previously presented) The wafer track system as recited in claim 48, wherein the distance between the first main wafer transporter and each of the process modules within its respective wafer processing stacks is substantially equal.